

1 **What is claimed is:**

1 1. A method of reducing the pattern effect in the
2 CMP process, comprising the steps of:

3 (a) providing a semiconductor substrate having a
4 patterned dielectric layer, a barrier layer
5 over the patterned dielectric layer, and a
6 conductive layer over the barrier layer;

7 (b) performing a first CMP process to remove part of
8 the conductive layer before the barrier layer
9 is polished, thereby a step height of the
10 conductive layer is reduced;

11 (c) depositing a layer of material substantially the
12 same as the conductive layer over the
13 conductive layer; and

14 (d) performing a second CMP process to expose the
15 patterned dielectric layer.

1 2. The method as claimed in claim 1, wherein the
2 conductive layer comprises copper or copper alloy.

1 3. The method as claimed in claim 1, wherein the
2 patterned dielectric layer comprises silicon dioxide,
3 silicon nitride, phosphosilicate glass,
4 borophosphosilicate glass, or fluorosilicate glass.

1 4. The method as claimed in claim 1, wherein the
2 barrier layer comprises Ta, Ti, TaN, TiN, or WN.

1 5. The method as claimed in claim 2, wherein the
2 deposition of copper or copper alloy is performed using
3 electroplating, CVD, or PVD.

1 6. The method as claimed in claim 1, wherein the
2 top surface of the remaining conductive layer after
3 performing the first CMP process is higher than the
4 barrier layer by more than 10Å.

1 7. The method as claimed in claim 6, wherein the
2 top surface of the remaining conductive layer after
3 performing the first CMP process is higher than the
4 barrier layer by from 100Å to 1000Å.

1 8. The method as claimed in claim 1, wherein the
2 top surface of the remaining conductive layer after
3 performing the first CMP process is approximately planar.

1 9. A method of eliminating dishing phenomena after a
2 CMP process, comprising the steps of:
3 providing a semiconductor substrate having a
4 patterned dielectric layer, a barrier layer
5 over the patterned dielectric layer, and a
6 conductive layer over the barrier layer;
7 performing a first CMP process to an end point of
8 polishing to remove part of the conductive
9 layer, wherein the dishing phenomena occur on
10 the conductive layer;
11 depositing a layer of material substantially the
12 same as the conductive layer over the
13 conductive layer; and
14 performing a second CMP process to expose the
15 patterned dielectric layer.

1 10. The method as claimed in claim 9, wherein the
2 conductive layer comprises copper or copper alloy.

1 11. The method as claimed in claim 9, wherein the
2 dielectric layer comprises silicon dioxide, silicon
3 nitride, phosphosilicate glass, borophosphosilicate
4 glass, or fluorosilicate glass.

1 12. The method as claimed in claim 9, wherein the
2 barrier layer comprises Ta, Ti, TaN, TiN, or WN.

1 13. The method as claimed in claim 10, wherein the
2 deposition of copper or copper alloy is performed using
3 electroplating, CVD, or PVD.

1 14. The method as claimed in claim 9, wherein the
2 top surface of the layer deposited in the step of
3 depositing a layer of material substantially the same as
4 the conductive layer over the conductive layer is higher
5 than the barrier layer.

1 15. A CMP rework method, comprising the steps of:
2 providing a semiconductor substrate which is
3 reported by a CMP machine as an abnormally
4 polished wafer at a predetermined CMP end point
5 and has a patterned dielectric layer, a barrier
6 layer over the patterned dielectric layer, and
7 a conductive layer over the barrier layer;
8 depositing a layer of material substantially the
9 same as the conductive layer over the
10 conductive layer; and

11 performing a CMP process to expose the patterned
12 dielectric layer.

1 16. The method as claimed in claim 15, wherein the
2 conductive layer comprises copper or copper alloy.

1 17. The method as claimed in claim 15, wherein the
2 dielectric layer comprises silicon dioxide, silicon
3 nitride, phosphosilicate glass, borophosphosilicate
4 glass, or fluorosilicate glass.

1 18. The method as claimed in claim 15, wherein the
2 barrier layer comprises Ta, Ti, TaN, TiN, or WN.

1 19. The method as claimed in claim 16, wherein the
2 deposition of copper or copper alloy is performed using
3 electroplating, CVD, or PVD.

1 20. The method as claimed in claim 15, wherein the
2 top surface of the layer deposited in the step of
3 depositing a layer of material substantially the same as
4 the conductive layer over the conductive layer is higher
5 than the barrier layer.